Amendments to the Specification:

At page 6, paragraph 1, please insert the following paragraph:

Figures 5A-D illustrates exemplary acts of forming electromechanical devices according to certain embodiments of the invention;

At page 6, paragraph 2, please insert the following paragraph:

Figures ~~6-8~~ 6A1 through 8B3, collectively, illustrate more particular acts of forming electromechanical devices according to certain embodiments of the invention;

At page 6, paragraph 3, please insert the following paragraph:

Figures 9A-D illustrates exemplary acts of forming electromechanical devices according to certain embodiments of the invention;

At page 6, paragraph 5, please insert the following paragraph:

Figures ~~13-18~~ 13A1-18B3, collectively, illustrate more particular acts of forming electromechanical devices according to certain embodiments of the invention.

At page 10, last paragraph, please insert the following paragraph:

Figures 5A–D illustrates a method of making certain embodiments of NTRCM devices 100. A first intermediate structure 500 is created or provided as explained in the incorporated patent applications, cited above. The structure 500 includes a silicon substrate 502 having a gate dielectric layer 504 (such as silicon dioxide) and an insulating support layer 506 (such as spin-on-glass (SOG)) that contains a plurality of supports 508. In this instance, the supports 508 are formed by rows of patterned insulating material, though many other arrangements are possible, such as a plurality of columns.

At page 13, paragraph 1, please insert the following paragraph:

Three possible methods for generating the upper intermediate structure 526 are described in connection with ~~figures 6A-B, Figures 7A-B, and Figures 8A-B.~~ Figures 6A1 through 8B3.

At page 13, paragraph 2, please insert the following paragraph:

Figures ~~6A-B~~ 6A1 through 6B3 show one approach for producing a three-trace structure 542. A lower intermediate structure 524 is provided or constructed using the techniques identified above. A sacrificial layer 602 (about 10-20 nm high) and an n-doped silicon layer 604 are then added using a CVD process, sputtering, electroplating, or a different deposition process.

At page 13, paragraph 5, please insert the following paragraph:

The resulting intermediate structure 540 is then processed so that the lower and upper sacrificial layers 518 and 534, respectively, are removed to result in structure 542, as discussed above in connection with figures 5A-D.

At page 13, paragraph 6, please insert the following paragraph:

Figures ~~7A-B~~ 7A1 through 7B3 show another approach for producing a three trace structure 542. A lower intermediate structure 524 like that described in connection with Figures 5A-D is provided or constructed. A sacrificial layer 702 (about 10-20 nm high) can be selectively grown directly above the underlying sacrificial layer 518, e.g., by using a selective CVD process involving self-complementary materials such as titanium, to produce intermediate structure 700. The resulting cavities 704 are filled and covered with a planar layer 708 of an insulating material such as spin-on-glass (SOG) or polyimide. The insulating layer 708 is backetched with RIE or a plasma to a height 710 equal to the intended total height of the upper sacrificial layer 702 and the upper conductive electrodes 724. A photoresist layer may be spin-coated on layer 708 and subsequently exposed and lithographically developed to create cavities which lie directly over the underlying electrodes 510.

At page 14, paragraph 1, please insert the following paragraph:

As illustrated by Figure ~~7B~~ 7B1 through 7B3, reactive ion etching (RIE) or the like may then be used to etch the upper support layer 708 to form cavities 714 and to define the upper supports 716. The cavities 714 are filled and covered with a planar layer consisting of n-doped silicon or other suitable electrode-forming materials, and this layer is backetched with RIE or a plasma to the same height 710 as the remaining portions of the support layer 722, the result being

intermediate 718. The top surfaces of the upper electrodes 724 and the supports 722 form a planar surface 726. A gate dielectric layer 730 is deposited on top of intermediate structure 718 to separate the upper electrodes 724 from the upper electrical ground conductive layer 732 (e.g., silicon), which is added on top of the gate dielectric layer. This results in structure 540 like those described above. Layer 732 serves the additional purpose of providing a hermetic seal covering the entire memory structure.

At page 14, paragraph 2, please insert the following paragraph:

The resulting intermediate structure 540 is then processed so that the lower and upper sacrificial layers 518 and 534, respectively, are removed to result in structure 542, as discussed above in connection with figures 5A-D.

At page 14, paragraph 3, please insert the following paragraph:

Figures ~~8A-B~~ 8A1 through 8B3 show another approach for producing a three trace structure 542. Intermediate structure 700 (as explained above) is provided or created. Under this approach, though, the cavities 704 are filled with n-doped silicon or other suitable electrode-forming materials to form a planar layer 804. The electrode layer 804 is backetched with RIE or a plasma to approximately the same height 710 as previously described. A photoresist layer may be spin-coated on layer 804 and subsequently exposed and lithographically developed to begin the creation of cavities 808 which lie directly over the underlying supports 508.

At page 14, paragraph 4, please insert the following paragraph:

As illustrated in 8B1 through 8B3, reactive ion etching (RIE) or the like may then be used to complete the cavities 808 and to define the upper electrodes. The cavities 808 of intermediate 806 are then filled and covered with a planar insulating layer, consisting, for example, of SOG or polyimide. The insulating layer is backetched with RIE or a plasma to form the supports 722 with a height 710 equal to the total height of the upper sacrificial layer 702 and the upper silicon electrodes 724. The result is intermediate structure 718, with a flat surface 726 as previously described. Substrate 718 is converted into substrate 728 by adding gate dielectric and upper electrical ground layers as described above.

At page 15, paragraph 1, please insert the following paragraph:

The resulting intermediate structure 540 is then processed so that the lower and upper sacrificial layers 518 and 534, respectively, are removed to result in structure 542, as discussed above in connection with figures 5A-D.

At page 15, paragraph 3, please insert the following parargraph:

Figures 9A-D illustrates a method of making these "shifted" embodiments of NTRCM devices. A first intermediate structure 500, as described above, is created or provided. Structure 500 is then converted, as described above, to intermediate 524 featuring patterned nanotube ribbons 522 on top of intermediate 500. Upper insulating supports 902 are deposited onto the lower supports 508, and upper sacrificial layers 904 having the same height as the upper supports 902 are deposited on top of ribbons 522 but in alignment with the lower sacrificial layers 518, so as to create a flat surface 906. The height of the upper sacrificial layers 904 and upper supports 902 is approximately the same as the height of the lower sacrificial layer 518, e.g., 10-20 nm on average. The upper supports 902 and upper sacrificial layers 904 may be made of the same materials as the corresponding lower layers but are not limited to these materials.

At page 16, paragraph 4, please insert the following parargraph:

Figures ~~13A-B~~ 13A1 through 13B3 show one approach for producing a three-trace structure 912. A lower intermediate structure 524 is provided or constructed using the techniques identified above. A support layer 1302 of about the same height as the lower sacrificial layer 518 is deposited to generate intermediate structure 1300. The layer 1302 is then patterned by photolithography and etching techniques, such as RIE, to create the supports 902 and to define cavities 1306 of intermediate structure 1304.

At page 17, paragraph 1, please insert the following paragraph:

The upper and lower sacrificial layers 904 and 518 are then removed, as explained in conjunction with Figures 9A-D, to generate the freely suspended, tristable nanotube junctions 914 of the target structure 912.

At page 17, paragraph 2, please insert the following paragraph:

Figures ~~14A-B~~ 14A1 through 14B3 show another approach for producing a three-trace structure 912. Intermediate structure 524 is provided or created and then transformed into intermediate 1400 by evaporation onto its surface of an upper sacrificial layer 1402 of about the same height as the lower sacrificial layer 518. This sacrificial layer is then patterned by lithography and etching to form sacrificial layer lines 1406 separated by cavities 1408 of intermediate 1404.

At page 17, paragraph 3, please insert the following paragraph:

The cavities 1408 are then filled by a flat layer of support material which is backetched to the same height as the sacrificial layer lines 904 to form a flat surface 906 and to form intermediate structure 1310. Intermediate 1310 is converted into intermediate 900 as explained in conjunction with Figures 13B1-13B3. The upper and lower sacrificial layers 904 and 518 are removed to form the target structure 912 containing freely suspended, tristable nanotube junctions 914.

At page 17, paragraph 4, please insert the following paragraph:

Figures 15A-D shows another approach for producing a three-trace structure 912. First, support layers 902 (about 10-20 nm high) are selectively grown on top of the lower structure 524 directly above the lower supports 508, e.g., by using a selective CVD process involving self-complementary materials such as titanium or silicon dioxide. The resulting intermediate 1304 is then converted successively into intermediate 1310, intermediate 900, and finally the target structure 912, as described above in conjunction with Figures 13B1-13B3.

At page 17, paragraph 5, please insert the following paragraph:

Figures 16A-E shows another approach for producing a three-trace structure 912. Sacrificial layers 904 are selectively deposited on the lower array 524 to form intermediate 1404. Intermediate 1404 is then converted via intermediates 1310 and 900 into the target structure 912, as described above in conjunction with Figures 14B1-14B3.

At page 18, paragraph 1, please insert the following paragraph:

Figures 17A-17E shows another approach for producing a three-trace structure 912. Intermediate 524 is created or provided. A sacrificial layer 1402, made of the same material as the lower sacrificial layer 518, and an electrode layer 1702 are deposited to form structure 1700. The electrode layer 1702 is then patterned by lithography and RIE to form electrode lines 908. Subsequently, the exposed part of the upper and lower sacrificial layers are removed by RIE to form intermediate 1706. The remaining sacrificial material 1708 is located only underneath the electrode lines 908. Where sacrificial material was removed, the now freely suspended nanotube ribbons form junctions 1710 with a freely suspended length, in the embodiment pictured (in which array elements are assumed to have been made as small as possible), of approximately half the resolution limit of the lithography used for patterning.

At page 18, paragraph 3, please insert the following paragraph:

Figures ~~18A-B~~ 18A1 through 18B3 illustrate yet another approach for producing a three-trace structure 912. Intermediate 1800 is produced by evaporating a sacrificial layer 1802 and an electrode material layer 1702 onto intermediate 524. The upper sacrificial layers 1802 are made of a material that has different etching characteristics than the lower sacrificial layers 518.

At page 18, paragraph 4, please insert the following paragraph:

The electrode material layer 1702 is patterned to form the electrode lines 908 of intermediate 1804. Subsequently, the exposed region of the sacrificial layer 1802 in between electrodes 908 is removed by RIE to form intermediate 1806 of Figures 18B1-18B3. Then the lower sacrificial layer 518 is removed by etching to form intermediate 1808. The remaining portions 1810 of the upper sacrificial layers directly above the lower electrodes 510 are removed by utilizing their higher differential solubility compared to the portions 1812 of sacrificial material directly above the lower supports 508. Because sacrificial material 1810 directly above the lower electrodes is much more easily accessed than sacrificial material 1812 directly above the lower supports, the material directly above the lower electrodes etches faster. Thus, by applying etchant but stopping the etching process at the appropriate time, the freely suspended, tristable junctions 914 of the target structure 1814 can be generated.